C. U. SHAH UNIVERSITY – WADHWAN CITY

FACULTY OF TECHNOLOGY AND ENGINEERING
DEPARTMENT OF COMPUTER ENGINEERING
B. TECH. SEMESTER: - III

SUBJECT NAME: - Digital Electronics (DEL)   **SUBJECT CODE: - 4TE03DEL1**

Teaching & Evaluation Scheme: -

Subject Code	Subject Name	Teaching Scheme (Hours)				Credits	Evaluation Scheme							Total
							Theory				Practical (Marks)			
		Th	Tu	Pr	Total		Sessional Exam		University Exam		Internal		University	
							Marks	Hours	Marks	Hours	Pr/Viva	TW	Pr	
4TE03DEL1	Digital Electronics (DEL)	4	0	2	6	5	30	1.5	70	3.0	30	20	-	150

Objectives: -
- The objective of the subject is to provide detailed knowledge on different number systems and codes, logic circuits, logic families and types of memories.

Prerequisites: Basic knowledge of mathematics and electronic circuits.

Course Outlines: -

Sr. No.	Course Contents	Total Hours
1	**Number System and codes:** Decimal, Binary, Octal, Hexa-decimal number system, Conversion of numbers from one number system to other, complement method of subtraction, 1's and 2's complement method,.8421 BCD code, excess-3 code, Gray code, Binary to Gray conversion, Gray to Binary conversion, Parity bit and its importance in error detecting.	**10**
2	**Logic Gates and Boolean Algebra:** AND, OR, NOR, NOT, NAND, X-OR, Inhibit circuits, Axioms and laws of Boolean algebra, D'morgans theorem, Duality, Reduction of Boolean expression, converting AND/OR/INVERT logic to NAND/NOR logic.	**08**
3	**Simplification of Boolean expression:** Expansion of a Boolean expression to SOP and POS form, Minimization of POS and SOP expressions for 2 to 6 variables, K-Map: 2, 3, 4 Variable, Don't care conditions, Quine-Mcclusky methods.	**09**
4	**Combinational Logic:** The Half-adder, The Full-adder, The Half-subtractor, The Full-Subtractor, Parallel Binary Adders, The Look-Ahead Carry Adder, Two's Complement Addition And Subtraction Using Parallel Adders, Serial Adders, BCD adder, Binary Multipliers, Code converters, Parity bit Generators/Checkers, Comparators, Decoders, BCD to 7-Segment Decoders, Encoders, Priority Encoders, Multiplexers, Applications of Multiplexer, Demultiplexer	**10**
5	**Sequential Logic:** S-R Flip-flop, JK Flip-flop, D Flip-flop, T Flip-flop, Edge –Triggered Flip-flop, Master-slave Flip-flop, Applications of Flip-flops. Serial-in Serial-out Shift register, Serial-in Parallel-out	**10**

	Shift register, Parallel-in Serial-out Shift register, Parallel-in Parallel-out Shift register, Bi-directional shift register, Universal shift register, Applications of shift registers. Asynchronous counter, Design of Asynchronous counter, Synchronous counters, Design of Synchronous counter.	
6	**Logic Families:** Digital IC specification terminology, Logic families, TTL, Open collector gate, TTL subfamilies, IIL , ECL, MOS, CMOS, Dynamic MOS Logic	**07**
7	**Memories :** Memory types and terminology, Read Only memory, Semiconductor RAMs, Non-volatile RAMs, Sequential memories, Programmable logic Devices, Magnetic memories, Optical Disk memory, Charge coupled devices.	**06**

Learning Outcomes: -

After successful completion of the course students will be able to:

- Understand the various number systems and codes.
- Understand the basics of various digital circuits such as combinational and sequential logic circuits
- Understand different logic families such as TTL, DTL, ECL etc.
- Understand different types of memories.

Books Recommended:-

1. "Digital logic and computer Design", **M. Morris Mano**, PHI Publication
2. "Fundamentals of Digital Circuits", **A. Anandkumar**, PHI Publication
3. "Digital Electronics", **R .P. Jain**, TMH Publication
4. "Digital Electronics and Logic Design", **B. Somanathan Nair**, PHI publication